Ahmad Shabani

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08 Jul 1992

PROFILE

Ahmad Shabani is an expert in *Hardware Security and Trust*, *Low-Power & High-Speed VLSI Circuits*, and *Digital ASIC Design*. With a PhD in digital electronic systems from the University of Tehran, he currently serves as an adjunct instructor at both the University of Tehran and Amirkabir University, where he shares his expertise with students. Ahmad's research primarily focuses on developing efficient countermeasures against Hardware Trojans, employing both pre and post-silicon detection techniques. Additionally, he is also proficient in digital Integrated Circuit (IC) design, covering both front-end and back-end stages of digital ASIC design flow. His research and academic contributions have been recognized through numerous publications in prestigious journals and conferences, as well as by receiving esteemed awards and prizes. These achievements not only highlight his significant contributions to advancing the field of hardware security but also underscore his dedication to excellence.

EDUCATION

2016 – 2021
Tehran, Iran

Ph.D.: Digital Electronic Systems
University of Tehran
GPA: (18.02 Out of 20)
Ph.D. Dissertation: "Hardware Trojan Detection Approaches Using Design for Hardware Trust"; (Score: **Excellent**)
Goal: Design efficient methodologies based on Design for Hardware Trust (DfTr) to detect hardware Trojans mounted by untrusted foundry. To do so, a modified hardware with minor design overheads and a compact set of test-vectors are proposed to facilitate the post-silicon Trojan detection and shorten the evaluation time.

2014 – 2016
Tehran, Iran

MSc: Digital Electronic Systems
Shahid Beheshti University
GPA: (19.37 Out of 20)
MSc Dissertation: "Design and Implementation of Low-Power Discrete Cosine Transform Using CORDIC Algorithm"; (Score: **Excellent**).
Goal: Design and implement a low-power DCT architecture by substituting massive multipliers with simple shift and add units based on CORDIC algorithm for battery-based application including Wireless Capsule Endoscopy (WCE) and compressor engine in emerging High Efficiency Video Coding (HEVC).

2010 – 2014
Shiraz, Iran

BSc: Electrical Engineering - Electronics
Shiraz University
GPA: (16.50 Out of 20);
BSc Project: "Simulating Fiber Optic Sensors With Modified Cladding Based on Maxwell's Equations"; (**Score:** Excellent).

HONORS & AWARDS

Recipient of Prestigious Award for Outstanding Ph.D. Dissertation.
19th International ISC Conference on Information Security and Cryptography (ISCISC2022), 2022

Ranked 1st Among Graduate Students in Master's Degree Program.
Shahid Beheshti University, Digital Electronic Systems, Tehran, IRAN, 2016.

Recipient of Student Prize from Iran's National Elites Foundation.
Recipient of Student Prize for two successive years, Iran's National Elites Foundation, 2017-2018.

Guest Speaker at the International ISC Conference on Information Security and Cryptology (ISCISC2023)
Presenting a speech titled "Empowering Hardware Security Through CAD Tools for Hardware Trojan Detection" Iranian Society of Cryptology, 2023.

Admitted to Ph.D. Degree Program with Exceptional Merit, Waiving Entrance Exam Requirement.
Organization for Development of Exceptional Talents, University of Tehran, Tehran, Iran, 2016.

Top-Ranked Student in High School, Demonstrating Academic Excellence.
Consistently Recognized as a Top-Ranked Student at Motahari High School for Three Consecutive Years (2008-2010).

RESEARCH PROJECTS

National Project for Monitoring and Management of Water and Wastewater Based on IoT Ecosystem
Niroo Research Institute, Smart Grid Center, Tehran, Iran, 2018-2019.

Supervisor of project "Investigating the Communication and Security Considerations of Smart Power Grid
Niroo Research Institute, Smart Grid Center, Tehran, Iran, 2019.

Evaluate Security Measures in Distributed Management System (DMS) for Smart Grid.
Iran's National Elites Foundation, University of Tehran, Iran, 2020.

TEACHING EXPERIENCE

2023 – present
Tehran, Iran

Adjunct Instructor at Amirkabir University of Technology (Tehran Polytechnique)
Course: "Computer Architecture" RISC-V Edition
Description: Designed to provide students with a fundamental understanding of the principles and concepts underlying the design and organization of computer systems. This course will initially start with the basic computer with simple ISA, and extend to RISC-V computer to introduce more advanced topics.

2021 – 2023
Tehran, Iran

Adjunct Instructor at University of Tehran
Course: "Core-Based Embedded System Design"
Description: Understanding the fundamental concepts and features of embedded systems. Each chapter present a different component of embedded systems in detail including processors and microcontrollers (Mainly RISC-V), memories, communication protocol, and sensors and actuators.

2015 – 2016
Tehran, Iran

Teacher Assistance (TA) at Shahid Beheshti University
Course: Electronics II

2014 – 2015
Shiraz, Iran

Teacher Assistance (TA) at Shiraz University
Course: "Electronics II"

2013 – 2014
Shiraz, Iran

Teacher Assistance (TA) at Shiraz University
Course: "Electronics I"

PROFESSIONAL EXPERIENCE

2023 – present
Tehran, Iran

Automotive Engineer & Hardware Expert
Azin Elctro Idea
- Working on the communication protocols and security measures in Passive-Entry Passive Start (PEPS) system.
- System-level design and supervising the board-level design for smart electronic module in cars.

2022 – 2023
Tehran, Iran

Digital ASIC Designer
Mana Excellence Center
- Manager of Digital ASIC Design of Automotive-Graded ICs;
- Collaboration in system-level Design and RTL description using VHDL/ Verilog;
- Participation in synthesis, simulation, LEC, coverage estimation, and static timing analysis (STA);
- Close collaboration with Analogue guys to better define partitioning, interfaces, and constraints for mixed-signal components;
- Participation in physical design including partitioning, floorplanning, power planning, placement, CTS, and routing;
- Collaboration in Sign-off & Silicon proof stage including Post-P&R STA, DRC, LVS, ERC, PEX, IR drop, and power-rail analysis

2020 – 2022
Tehran, Iran

Chief Technology Officer (CTO)
Shahab Co
Head of the electronic department working on:
- Design non-destructive & low-cost smart electricity meters based on IoT including the hardware and firmware parts;
- Developing small-sized devices including hardware and firmware to monitor non-smart gas meters using computer vision and image processing on the edge;

2018 – 2020
Tehran, Iran

IoT Expert & Hardware Security Specialist
Niroo Research Institute - Smart Grid Center-
IoT specialist working on:
- Research on IoT trends, projects, and challenges in the energy sector including water and wastewater management, smart agriculture and irrigation, the oil and gas industry, and the power industry;
- Research on IoT security issues and solutions in the energy sector;

PROJECTS (ASIC, HW, SW)

"Digital ASIC Design (Front-End & Back-End) of High-Speed and Fault-Tolerant CAN Transceivers" Mana Excellence Center, 2022-2023.
Designing the digital part of high-speed and fault-tolerant CAN transceiver IC.

Digital ASIC Design (Verification and Back-End) of Immobilizer IC Used in Automotive Key-Fobs, Freelance Project, 2023.
Designing the digital part of Transponder IC available in automotive Key-Fobs

"Digital ASIC Design (Front-End & Baqck-End) of SPI-Based Smart Switch Detector" Mana Excellence Center, 2022-2023.
Designing the digital part of a smart switch detector based on SPI protocol with configurable wetting current, termination node, analog output, and can receive the switch status as a response.

"Digital ASIC Design (Front-End & Back-End) of LIN Transceiver"
Mana Excellence Center, 2022-2023.
Designing the digital part of LIN transceiver.

"Smart Electricity Meter (Harware & Firmware Development)"
Shahab-Co, 2021-2022.
Low-cost non-destructive ESP-based smart electricity meter able to measure energy, voltage, and current of twelve input channels, and send them to the server in real-time using WiFi. For more info visits (https://github.com/hiddenman23?tab=repositories).

"Gas Meter Telemetry Add-on Based on Computer-Vision"
Shahab-Co, 2021-2022.
A small-sized device capable of adding telemetry and supervised monitoring to the traditional non-smart gas meters. The device incorporates a low-cost camera and can process the image taken from the gas meter, extract the digits (locally or server-side), and send the result to the server via WiFi.

PUBLICATIONS (SEE SCHOLAR PROFILE)

A Sajadi, A Shabani, B Alizadeh; "*DC-PUF: Machine learning-resistant PUF-based authentication protocol using dependency chain for resource-constraint IoT devices*", Journal of Network and Computer Applications, 2023.

Ashtari, Amir, Ahmad Shabani, and Bijan Alizadeh. "Mutual Lightweight PUF-Based Authentication Scheme Using Random Key Management Mechanism for Resource-Constrained IoT Devices." ISeCure 14.3 (2022).

Khormizi, Fatemeh, Ahmad Shabani, and Bijan Alizadeh. "*Hardware Patching Methodology for Neutralizing Timing Hardware Trojans Using Vulnerability Analysis and Time Borrowing Scheme*." IEEE Transactions on Circuits and Systems II: Express Briefs (2022).

Ashtari, Amir, and Bijan Alizadeh. "A comparative study of machine learning classifiers for secure RF-PUF-based authentication in internet of things." Microprocessors and Microsystems 93 (2022): 104600.

M Sabri, A Shabani, B Alizadeh - "*SAT-Based Integrated Hardware Trojan Detection and Localization Approach Through Path-Delay Analysis",* IEEE Transactions on Circuits and Systems II: Express, 2021

Shabani, Ahmad, and Bijan Alizadeh. "*Enhancing hardware Trojan detection sensitivity using partition-based shuffling scheme*."IEEE Transactions on Circuits and Systems II: Express Briefs 68.1 (2020): 266-270.

Shabani, Ahmad, and Bijan Alizadeh. "*PODEM: A low-cost property-based design modification for detecting hardware trojans in resource-constraint IoT devices*." Journal of Network and Computer Applications 167 (2020): 102713.

Shabani, A., Sabri, M., Khabbazan, B., & Timarchi, S. (2020). "*Area and Power-Efficient Variable-Sized DCT Architecture for HEVC Using Muxed-MCM Problem*". IEEE Transactions on Circuits and Systems I: Regular Papers, 68(3), 1259-1268.

A. Shabani, B. Alizadeh; "*PMTP: A MAX-SAT Based Approach to Detect Hardware Trojan Using Propagation of Maximum Transition Probability*", Journal of Transaction of Computer Aided Devices (TCAD), 2019.

Ashtari, Amir, Ahmad Shabani, and Bijan Alizadeh. "A new RF-PUF based authentication of internet of things using random forest classification." In 2019 16th International ISC (Iranian Society of Cryptology) Conference on Information Security and Cryptology (ISCISC), pp. 21-26. IEEE, 2019.

A. Shabani, S. Timarchi, H. Madavi; *"Power and Area Efficient CORDIC-Based DCT Using Direct Realization of Decomposed Matrix*", Microelectronic Journal, 2019.

A. Shabani, S. Timarchi. "Low-power DCT-based compressor for wireless capsule endoscopy." Journal of Signal Processing: Image Communication, 2017

SKILLS

Hardware Security & Hardware Trojan
Preserve confidentiality, authentication, detection malicious modifications, PUF, logic testing, logic locking, and side-channel analysis.

Perl &TCL Programming
Familiar in writing CAD automation scripts

Synopsys PrimeTime
Experienced in static timing analysis for both pre and post-layout stages

Synopsys VCS
Functional verification solution

Cadence Innovus
Physical implementation tool

Calibre (DRC, LVS, PEX)
Post layout checking and netlist extraction

Sensors & Modules
Accelerator (MPU6050), OLED (1.3", 0.96"), Hall Effect (44E, AK09911C), IR, PIR (HC- SR501), ADC (MCP3008, ADS1115), RTC (PCF8563, PCF8523), WiFi (ESP-07, ESP-12E, ESP-12N), Light (GY-302)

Development Boards
ESP32CAM, ESP32 (WROOM-32), Arduino Uno/ Mega, NodeMCU, Raspberry Pi (ZeroW),

Programming Language
Perl, C/C++, Python, Fortran, CUDA, SystemC

Hardware Description Language (VHDL/Verilog)
Proficient in synthesizable hardware description

Synopsys Design Compiler
Synthesis, Optimization, Design Constraints, Power analysis, and Timing Analysis

Synopsys Formaility
Logic equivalence checking (LEC)

Mentor Graphics QuestaSim
efficient simulation tool for hardware description

Cadence Virtuoso
IC design/analysis, Co-simulation

Cadence Voltus & Quantus
IR Drop analysis & parasitic extraction tools

EDA & IDE
Proteus, Multisim, Orcad Pspice, Altium Designer, GHDL, Icarus Verilog, Quartus(Altera), ISE/Vivado Design Suite (Xilinx), CodeVision, Netbeans, VSCode, Atmel Studio.

Microcontroller & SOCs
ESP32, ESP8266, AVR (ATmega 8, 16, 32, 328), ATTiny85, STM32F103C8T6, NXP-LPC1788

System-Level design & Board-Level Design
Experienced in embedded hardware and software, schematic and PCB design for various application.

CAREER INTERESTS

Hardware Security; Hardware Trojans; PUF-Based Authentication, Low-Power & High-Speed VLSI Circuits; Embedded HW & SW Design.

REFERENCES

Dr. Somayeh Timarchi,
Associate Professor, Department of Electronics, Shahid Beheshti University, Tehran, Iran.
Email: s_timarchi@sbu.ac.ir

Dr. Bijan Alizadeh, *Associate Professor, Department of Electronics, University of Tehran, Tehran, Iran.*
Email: b.alizadh@ut.ac.ir

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Associate Professor, Department of Electrical and Computer Engineering, Jahrom University, Jahrom, Iran.
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